

## Publikationen

(2017): Empirical results on parity-based soft error detection with software-based retry. In: Microprocessors and Microsystems, vol. 48, no. February, pp. 62-68. DOI: 10.1016/j.micpro.2016.09.009.

(2016): Exploiting error detection latency for parity-based soft error detection. In: Proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) [Kosice, Slovakia] .

(2015): Parity-based Soft Error Detection with Software-based Retry vs. Triplication-based Soft Error Correction - An Analytical Comparison on a Flash-based FPGA Architecture. In: Informatik 2015 - Informatik, Energie und Umwelt (28.09.-02.10.2015; Cottbus), Bonn, vol. P-246.

(2015): In-circuit Error Detection with Software-based Error Correction - An Alternative to TMR. In: Formal Modeling and Verification of Cyber-Physical Systems.

(2015): Empirical results on parity-based soft error detection with software-based retry. In: Proceedings of the 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC) . DOI: 10.1109/NORCHIP.2015.7364378.

: Parity-based Error Detection with Recomputation for Fault-tolerant Spaceborne Computing.